Delhi Technological University

(Formerly Delhi College of Engineering) Consolidated Result Notification

Programme: Master of Technology

The following Candidates who appeared in Master of Technology-VLSI Design & Embedded System End Semester examinations held in MAY, 2025 have completed the requirement and hence declared to have pass the final examinations. These Candidates have obtained 58 or more credits.

Branch: VLSI Design & Embedded System Notification Number: 1861

Result Declaration Date: 2025-07-14

Sr. No.	Name	Roll No.	Name in Hindi	TC	CGPA
	CGPA - Cumulative Grade Point Average		TC - Total Credits		
1	BRIJ NANDAN SINGH	23/VLS/01	ब्रिज नंदन सिंह	58	8.88
2	SHASHI RANJAN UPADHYAY	23/VLS/03	शशिरंजन उपाध्याय	58	8.97
3	PRAKHAR SAINI	23/VLS/04	प्रखर सैनी	58	7.95
4	MOHAMMAD TALHA	23/VLS/05	मोहम्मद तल्हा	58	7.74
5	PRAJVI UDAR	23/VLS/06	प्राजवि उदार	58	8.26
6	MAYANK CHAUHAN	23/VLS/07	मयंक चौहान	58	7.84
7	AMARTYA ROY	23/VLS/08	अमर्त्य रॉय	58	7.67
8	DEEPTI	23/VLS/09	दीप्ति	58	7.72
9	AASTHA SINGH	23/VLS/10	आस्था सिंह	58	8.38
10	GAJJAR JAY UMESH BHAI	23/VLS/11	गजर जय उमेश भाई	58	7.90
11	PREETI	23/VLS/12	प्रीति	58	7.95
12	ASMAR HAFEEZ	23/VLS/13	असमर हफीज	58	7.47
13	TUSHANT VERMA	23/VLS/14	तुशांत वर्मा	58	7.74

OIC (Results) Controller of Examination

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Sr. No.	Name	Roll No.	Name in Hindi	TC	CGPA
	CGPA - Cumulative Grade Point Average		TC - Total Credits		
14	AKHILESH VISHWAKARMA	23/VLS/15	-अखिलेश विश्वकर्मा	58	7.40
15	RAMLAKHAN	23/VLS/16	रामलखन	58	7.67
16	DEVESH SAINI	23/VLS/17	देवेश सैनी	58	7.02
17	KUNCHA AKHILESH KUMAR	23/VLS/18	कुंचा अखिलेश कुमार	58	7.26
18	SOUMYAJIT DAS	23/VLS/19	सौम्यजीत दास	58	8.17
19	UJJWAL BHARTI	23/VLS/20	उज्जवल भारती	58	7.50
20	TVISHA PUSHKAR	23/VLS/21	टीवीशा पुष्कर	58	9.17
21	MANISH SINGH	23/VLS/23	मनीष सिंह	58	7.62
22	ADITYA RAYER	23/VLS/24	आदित्य रायर	58	7.76
23	YASHODA PARMAR	23/VLS/25	यशोदा परमार	58	9.09

OIC (Results)

Controller of Examination