



**Delhi Technological University**  
(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN MAY 2025 IS DECLARED AS UNDER:-

**Master of Technology(VLSI Design & Embedded System), II-SEMESTER**

Result Declaration Date : 12-08-2025

Notification No: 1872

VLS502n : Low Power VLSI Design VLS5323n : Advanced Computer Architecture

Sr.No	Roll No.	Name of Student	VLS502n	VLS5323n	SGPA	TC	Failed Courses
			4.00	4.00			
1	24/VLS/501	AYUSHI AGRAWAL	B+	O	8.50	8	
2	24/VLS/502	NISHITA BHARDWAJ	F	A	4.00	4	VLS502n

OIC (Results)

Controller of Examination

**Note:**Any discrepancy in the result in r/o name/roll no/registration/marks/grades/course code/title should be brought to the notice of Controller of Examination/OIC(Results) within 15 days of declaration of result, in the prescribed proforma.