



**Delhi Technological University**  
(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN NOV 2024 IS DECLARED AS UNDER:-

**Master of Technology(VLSI Design & Embedded System), I-SEMESTER**

Result Declaration Date : 12-08-2025

Notification No: 1872

VLS505 : Digital IC Design VLS507 : Semiconductor Devices and Modelling VLS509 : Digital Design with HDL

Sr.No	Roll No.	Name of Student	VLS505	VLS507	VLS509	SGPA	TC	CGPA	Failed Courses
			4.00	4.00	4.00				
1	24/VLS/501	AYUSHI AGRAWAL	B+	B+	A	7.33	12	7.33	
2	24/VLS/502	NISHITA BHARDWAJ	C	P	C	4.67	12	4.67	

OIC (Results)

Controller of Examination

**Note:**Any discrepancy in the result in r/o name/roll no/registration/marks/grades/course code/title should be brought to the notice of Controller of Examination/OIC(Results) within 15 days of declaration of result, in the prescribed proforma.