Delhi Technological University

(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN JULY 2025 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), I-SEMESTER

Result Declaration Date : 29-08-2025   **Notification No: 1883**

VLS507 : Semiconductor Devices and Modelling   VLS504n : Mixed Signal Design

Sr.No	Roll No.	Name of Student	VLS507 4.00	VLS504n 4.00	Failed Courses
1	24/VLS/23	SUBODH LAKRA	P	B	

OIC (Results)   **Controller of Examination**

Note: Any discrepancy in the result in r/o name/roll no/registration/marks/grades/course code/title should be brought to the notice of Controller of Examination/OIC(Results) within 15 days of declaration of result, in the prescribed proforma.