

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN NOV 2024 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), III-SEMESTER

Result Declaration Date: 19-04-2025 Notification No: 1813

VLS601: MAJOR PROJECT I

Sr.No	Roll No.	Name of Student	VLS601	SCDV	TC	Failed Courses	
			3.00	JUFA	'`	raileu Courses	
1	23/VLS/01	BRIJ NANDAN SINGH	0	10.000	3		
2	23/VLS/03	SHASHI RANJAN UPADHYAY	A+	9.000	3		
3	23/VLS/04	PRAKHAR SAINI	A+	9.000	3		
4	23/VLS/05	MOHAMMAD TALHA	A+	9.000	3		
5	23/VLS/06	PRAJVI UDAR	0	10.000	3		
6	23/VLS/07	MAYANK CHAUHAN	A+	9.000	3		
7	23/VLS/08	AMARTYA ROY	A+	9.000	3		
8	23/VLS/09	DEEPTI	A+	9.000	3		
9	23/VLS/10	AASTHA SINGH	0	10.000	3		
10	23/VLS/11	GAJJAR JAY UMESH BHAI	A+	9.000	3		
11	23/VLS/12	PREETI	A+	9.000	3		
12	23/VLS/13	ASMAR HAFEEZ	A+	9.000	3		
13	23/VLS/14	TUSHANT VERMA	A+	9.000	3		
14	23/VLS/15	AKHILESH VISHWAKARMA	A+	9.000	3		
15	23/VLS/16	RAMLAKHAN	A+	9.000	3		
16	23/VLS/17	DEVESH SAINI	0	10.000	3		
17	23/VLS/18	KUNCHA AKHILESH KUMAR	A+	9.000	3		
18	23/VLS/19	SOUMYAJIT DAS	A+	9.000	3		
19	23/VLS/20	UJJWAL BHARTI	A+	9.000	3		
20	23/VLS/21	TVISHA PUSHKAR	0	10.000	3		

OIC (Results)

Controller of Examination



(Formerly Delhi College of Engineering)

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	21	23/VLS/23	MANISH SINGH	A+	9.000	3	
Γ	22	23/VLS/24	ADITYA RAYER	0	10.000	3	

VLS601: MAJOR PROJECT I VLS6207: Selected topics in VLSI VLS6301: Speech Processing VLS6401: Mixed Signal Design

Sr.No	Roll No.	Name of Student	VLS601	VLS6207	VLS6301	VLS6401	SGPA	тс	Failed Courses
31.110	Holl No.	Name of Student	3.00	2.00	3.00	4.00		'C	
23	23/VLS/25	YASHODA PARMAR	0	0	Α	A+	9.167	12	

OIC (Results)

Controller of Examination