Delhi Technological University

(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN MAY 2026 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), IV-SEMESTER

Result Declaration Date : 17-Aug-2026 **Notification No: 1970**

UCC502n : Research Methodology VLS538n : Machine Learning in VLSI Design VLS546n : Analog and Digital Design Skills

Sr.No	Roll No.	Name of Student	UCC502n	VLS538n	VLS546n	SGPA	TC	Failed Courses
			4.00	4.00	4.00			
1	24/VLS/501	AYUSHI AGRAWAL	B+	C	B+	6.33	12	
2	24/VLS/502	NISHITA BHARDWAJ	B	C	B+	6.00	12	

OIC (Results) **Controller of Examination**

Note: Any discrepancy in the result in r/o name/roll no/registration/marks/grades/course code/title should be brought to the notice of Controller of Examination/OIC(Results) within 15 days of declaration of result, in the prescribed proforma.