Delhi Technological University

(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN MAY 2026 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), II-SEMESTER

Result Declaration Date : 21-Jul-2026

Notification No: 1968 (Revised on 12.08.2026)

UCC502n : Research Methodology VLS502n : Low Power VLSI Design VLS504n : Mixed Signal Design VLS524n : Advanced Computer Architecture VLS538n : Machine Learning in VLSI Design VLS546n : Analog and Digital Design Skills

Sr.No	Roll No.	Name of Student	UCC502n	VLS502n	VLS504n	VLS524n	VLS538n	VLS546n	SGPA	TC	Failed Courses
			4.00	4.00	4.00	4.00	4.00	4.00			
1	25/VLS/07	PRATYANCH JAIN	A	A	B+	A+	B	A+	7.83	24	
2	25/VLS/13	JUGMADEEP SAIKIA	A+	B	B+	A+	B+	A	7.67	24	

OIC (Results) **Controller of Examination**

Note: Any discrepancy in the result in r/o name/roll no/registration/marks/grades/course code/title should be brought to the notice of Controller of Examination/OIC(Results) within 15 days of declaration of result, in the prescribed proforma.